AF

OBLON
SPIVAK
MCCLELLAND
MAIER
&
NEUSTADT
P.C.

ATTORNEYS AT LAW

ECKHARD H. KUESTERS
(703) 413-3000
EKUESTERS@OBLON.COM

RAYMOND F. CARDILLO, JR.
(703) 413-3000
RCARDILLO@OBLON.COM

Docket No.: 249040US2S DIV

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/779,661
Applicant: Fumitomo MATSUOKA
Filing Date: February 18, 2004
For: SEMICONDUCTOR DEVICE AND A METHOD FOR MANUFACTURING THE SAME
Group Art Unit: 2815
Examiner: LEE, EUGENE

SIR:

Attached hereto for filing are the following papers:

APPEAL BRIEF

Our **credit card payment form** in the amount of **$500.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Registration No. 28,870

Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850
(703) 413-3000 (phone)
(703) 413-2220 (fax)

DOCKET NO: 249040US2S DIV

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
FUMITOMO MATSUOKA	: EXAMINER: LEE, E.
SERIAL NO: 10/779,661	:
FILED: FEBRUARY 18, 2004	: GROUP ART UNIT: 2815
FOR: SEMICONDUCTOR DEVICE AND A METHOD FOR MANUFACTURING THE SAME	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

The present Appeal Brief is submitted in response to the Final Rejection mailed August 4, 2006, and the Notice of Panel Decision mailed on December 13, 2006.

(i) REAL PARTY IN INTEREST

The real party in interest in the present appeal is KABUSHIKI KAISHA TOSHIBA having a place of business at 72 Horikawa-cho, Saiwai-ku, Kawasaki-shi, Japan.

(ii) RELATED APPEALS AND INTERFERENCES

Appellant, the appelant's legal representative, or assignee are not aware of any other prior or pending appeals, interference procedures, or judicial proceedings, that might directlyor indirectly affect or have a bearing on the Board's decision in the pending appeal.

(iii) STATUS OF CLAIMS

Claims 14, 15, 17, and 18 are pending in this application. Claims 1-13, 16, and 19 have been canceled. Claims 14, 15, 17, and 18 have been finally rejected and form the basis for the appeal. The attached claim appendix includes a clean copy of appealed Claims 14, 15, 17, and 18.

(iv) STATUS OF AMENDMENTS

No amendments have been filed after the final Action mailed August 4, 2006. A Request for a Pre-Appeal Brief Conference was filed with the Notice of Appeal on November 6, 2006, and a Notice of Panel Decision indicating the this application was to proceed to the Board of Patent Appeals and Interferences for a Decision as to the rejection of Claims 14, 15, 17, and 18 was mailed on December 13, 2006.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The subject matter of independent Claim 14 includes a semiconductor device shown in various manufacturing stages in FIGS. 9-15, for example, and as an exemplary insulated gate field effect transistor (hereinafter, MISFET) in FIG. 16, for example.

This MISFET device has a semiconductor substrate (301, for example) with spaced apart first and second impurity diffusion layers (309, illustrated on each side of the dummy gate 304 shown in FIG. 10, for example) that are formed therein. Tip portions (the extremes of portions 307, illustrated on each side of the dummy gate 304 shown in FIGS. 10 and 11, for example) are associated with each of the impurity diffusion layers and are also space apart by the dummy electrode 304. First and second insulating layer (311, illustrated on each side of the dummy gate 304 shown in FIG. 12, for example) are formed on the first and impurity diffusion layer so as to cover the first and second impurity diffusion layers without covering

the tip portions (the extreme end portions of extension regions 307 covered by 313 instead of 311, as illustrated in FIGS. 15 and 16, for example). A trench (312', for example) is formed over the semiconductor substrate between the first insulting layer and the second insulating layer (as illustrated in FIG. 14, for example) and a gate insulating film (313, for example) that contains one selected from the group consisting of Ta_2O5, Al_2O_3, $BaSrTiO_3$, Zr oxide Hf oxide, Sc oxide, Y oxide, and Ti oxide (as noted at page 16, lines 9-17, of the specification, for example) is lined on a bottom surface and an inner sidewall surface of the trench 312'(as illustrated in FIGS. 15 and 16, for example), and a gate electrode (314, for example) formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench, the gate electrode conductive layer (314, for example) being formed in an overlapped relation relative to the tip portion of the first impurity diffusion layer and the tip portion of the second impurity diffusion layer as emphasized by circled area 316 of FIG. 16, for example.

As noted at page 15, lines 9-12, of the specification, this "overlapped structure in which the end of the gate electrode overlaps the extensions 307 of the impurity diffusion layers 309" provides a MISFET of a stabler operation." Also, note the description of this MISFIT that operates stably despite the use of a high dielectric constant film as the gate insulating film at page 17, lines 8-23, of the specification.

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds for rejection to be reviewed on appeal and outstanding in the present application are as follows:

Claims 14, 15, 17, and 18 stand finally rejected under 35 U.S.C. §102(e) as being anticipated by Xiang et al. (U.S. Patent No. 6,159,782, Xiang).

(vii) ARGUMENT

A. The rejection of Claim 14,15, 17, and 18 under 35 U.S.C. §102(e) as being anticipated by Xiang

It is noted that this rejection as to parent independent Claim 14 is apparently at least in part based on the Examiner's interpretation of FIG.12B at page 3 of the outstanding final Action. Appellants note that the word "apparent" must be used as the explanation of this rejection (in paragraph 3 bridging pages 2 and 3 of the outstanding final Action) and the "Response to Arguments" (on the bottom of page 3 of this outstanding final Action) both fail to address all of Appellants arguments presented in the Amendment filed May 24, 2006 and to explain how the PTO is suggesting that the disclosure of FIG. 12B alone can be said to an accurate and precise showing of the positioning of the protrusions of the source and drain regions with regard to the overlying structures including spacers 168, the gate electrode layers (234, 254), the gate opening 214, the high dielectric constant layer 225, and the nitrided oxide layer 224.

In this regard, the above-noted paragraph 3 of the outstanding final Action first states that the p-well158 shown in this FIG. 12B is being read as the Claim 14 required device substrate, that drain 154 and source 156 are being read as the first and second impurity diffusion layers and that "168/204, spacers/insulator material" on each side of metal contact 254 are being interpreted to correspond to the Claim 14 recited first and second insulating layers. It then states that col. 6, lines 50-52 of Xiang "discloses the high dielectric constant being Ta_2O_5," and that col. 5, lines 28-30 and col. 6, line of Xiang "discloses the spacers and insulator material respectively comprising silicon dioxide." The "Response to Arguments" (on the bottom of page 3 of this outstanding final Action) simply emphasizes that this disclosure that the spacers and insulator material can both be made of silicon dioxide is relied upon to read elements 204, 168 on the left side of the gate electrode as the first insulating

layer and to read elements 204, 168 on the right side of the gate electrode as the second insulating layer.

However, there is no express statement of how the showings of FIG. 12B are relied upon to teach the limitation of Claim 14 requiring there to be "a tip portion opposite to the second impurity diffusion layer" and "a tip portion opposite to the first impurity diffusion layer," with both these tip portions being overlapped by the gate electrode conductive layer without any overlap by the respective first and second impurity diffusion layers.

Even though no express statement has been made, the reproduction of FIG. 12B at the top of page 3 of the outstanding final Action appears to imply that these parent Claim 14 recited "tip portions" are being equated to the extreme ends of the portions of drain 154 and source 156 that are labeled by the hand written notation "3rd," as at least the very ends of these "3rd" portions are **ILLUSTRATED** to be under the gate electrode structure (234, 254) and not under "168/204, spacers/insulator material" being interpreted to correspond to the recited first and second insulating layers. To the extent that the PTO is relying on this FIG 12B showing to teach the Claim 14 recited "tip portion opposite to the second impurity diffusion layer" and "tip portion opposite to the first impurity diffusion layer," with both of which must be overlapped by the gate electrode conductive layer without any overlap by the respective first and second impurity diffusion layers, it must is further be relying on this FIG 12B showing to be accurate and precise as to the relative sizes and positions of all of these illustrated elements.

The error in this approach is that it presumes that each of the source/drain (154/156) regions the Examiner has labeled as 3rd and 4th are drawn to at least the same horizontal scale as the layers 204,168, 224, 225, and 234, 254. However, nothing is stated by Xiang as to using such a common horizontal scale and nothing is suggested as a purpose for spacers 168 other that the purpose well understood by those of ordinary skill in the art as to the use of

spacers 168 to form lightly doped shallow portions (labeled 3rd in the FIG. 12B reproduction by the PTO) that are less deep than the main source/drain regions (labeled 4th in the FIG. 12B reproduction by the PTO).

1. The drawings of Xiang are not to scale and not of such a character to indicate that they are accurate as to relative sizes and positions of the elements illustrated therein.

Turning first to the lack of any disclosure by Xaing even suggesting that there is any reason to believe that there is any common scale (horizontal, vertical, or otherwise) being used in any Figure, this is clear from the actual statement in Xiang specifically pointing out (at col. 4, lines 46-47) that "[t]he figures referred to herein are drawn for clarity of illustration and are not necessarily drawn to scale" (emphasis added). Clearly, presumptions made that the relative size of any part of regions 154, 156 has a specific positional and size relationship to any part of spacers 168 and/or gate layers 252, 254, is contrary to this disclaimer that "[t]he figures referred to herein are drawn for clarity of illustration and are not necessarily drawn to scale" (emphasis added).

As noted by the PTO reviewing court in *Hockerson-Halberstadt, Inc. v. Avia Group. Int'l, Inc.*, 222 F.3d 951, 956, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000), "patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue." In addition note *In re Wright*, 569 F.2d 1124, 1127, 193 USPQ 332, 335 (C.C.P.A. 1977) ("Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value. *In re Chitayat*, 56 CCPA 1343, 408 F.2d 475, 161 USPQ 224 (1969)").

In re Wilson, 312 F.2d 449, 454, 136 USPQ188, 192, (CCPA 1963) is also relevant as to specifically pointing out that because "[p]atent drawings are not working drawings," arguments predicated on portions of drawings "obviously never intended to show the

dimensions of anything," like the apparent reliance on the size and positions of the ends of the labeled 3rd parts of diffusion regions 154, 156 relative to gate layers 234, 254 and spacers 168 of FIG. 12B of Xiang are without merit.

Thus, the situation here is like that in the above noted decisions and unlike the situation in various decisions that have found the drawings standing alone to be considered an accurate, particular, and precise description without any further explanation in the specification. Note, for example, *In re Reynolds*, 443 F.2d 384, 389, 170 USPQ 94, 98 (CCPA 1971), in which the court found that the involved drawings there themselves suggested that reasons existed "for the relationships shown in the drawings." While the drawings involved in *Reynolds* were found to alone constitute a disclosure placing that invention in the hands of the artisan without the need for any additional explanation in the specification, the key factor there was the "geometric certainty" created by those drawing that does not exist here. Similarly, it was the very precise showing of the drawing at issue in *In re Mraz*, 455 F.2d 1069, 1072, 173 USPQ 25, 27 (CCPA 1972) that led to the conclusion there that the involved reference drawing was sufficient without a description in the specification because it focused on the elements of concern there and showed "them with great particularity" (emphasis added), circumstances not present here.

2. There is nothing is suggested as a purpose for spacers 168 other that the purpose well understood by those of ordinary skill in the art as to the use of spacers 168 to form lightly doped shallow portions (labeled 3rd in the FIG. 12B reproduction by the PTO).

There is no teaching in Xiang as to any method to use to form the reduced depth parts of source/drain regions 154, 156 in a manner to insure that they will be overlapped by the gate electrode conductive layer. Also, there is no disclosure of any purpose for spacers 168 of Xiang (120 in the "A" Figures). The only reasonable conclusion under these circumstances is

that the spacers 168 of Xiang (120 in the "A" Figures) exist for the purpose of forming the shallow protruding portions of the source and drain regions beneath these sidewalls in the same manner as in background art FIGS. 1-8 of the present Application and the showings of FIGS. 1-10 of Gardner et al. (U.S. Patent No. 6,200,865, of record), for example. Note FIGS. 1-3 of Gardner et al. and background art FIGS. 1-2 of the present Application in particular as to forming shallow first diffusion regions without the presence of spacers that is followed by adding spacers to mask parts of these shallow first diffusion regions. After forming the spacers as masks, deeper second diffusion regions are formed as to portions of the shallow first diffusion regions that are not masked by the spacers. This process (illustrated by both FIGS. 1-3 of Gardner et al. and background art FIGS. 1-2 of the present Application) results in the spacers being directly over and aligned with the edges of the lightly doped regions, not the exaggeration of all the Figures of Xiang in which no alignment between the edges spacers 168 (and 120 of the "A" Figures) and the edges of the shallow diffusion regions can be seen.

3. The position and size of spacers 168 relative to the position and size of the shallow lightly doped portions labeled 3rd in the FIG. 12B reproduction by the PTO is at best an ambiguous disclosure.

As noted above, the Figures of Xiang are described therein as only presented "for clarity of illustration." Thus, these drawings are at best ambiguous as to the exact relative placement of the "B" Figure showings of spacers 168 (120 in the "A" Figures) and the final conductive gate layers 234, 254 (232, 252 in the "A" Figures) lying over the shallow lightly doped parts of the source 156 (106 in the "A" Figures) and drain 154 (104 in the "A" Figures) impurity diffusion layers. It is well established that such ambiguous showings subject to different interpretations cannot be relied upon to establish anticipation. *See, In re Turlay*, 304 F.2d 893, 899, 134 USPQ 355, 360 (CCPA 1962). Also note the requirement that references

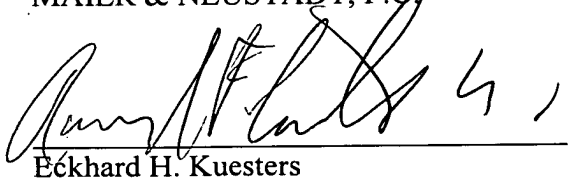
provide clear and definite disclosures as to the features therein that are being relied upon. See *In re Hughes*, 345 F.2d 184, 188, 145 USPQ 467, 471 (CCPA 1965) and *In re Moreton*, 288 F.2d 708, 711, 129 USPQ 227, 230 (CCPA 1961).

CONCLUSION

Applicant respectfully submits that the artisan would understand that FIGS 1-12 of Xiang are not intended to show the actual positions of the Xiang shallow source (106, 156) or shallow drain (104,154) lightly doped portions relative to either the spacers (120 or 168) or the final conductive gate electrodes 232, 252 or 234, 254. Further, Applicant respectfully submits that if these shallow lightly doped portions of the source (106, 156) and drain (104, 154) impurity diffusion layers were accurately depicted as to their exact locations relative to these spacers used to form them in the conventional manner, the showing would match the aligned background art FIG. 8 of this Application and the similar aligned showing of FIG. 3 of Gardner, for example, and would be subject to the problem that the present invention seeks to overcome and that is not recognized or discussed by Xiang. Thus, reversal of the outstanding rejection of Claims 14, 15, 17, and 18 d under 35 U.S.C. §102(e) as being anticipated by Xiang is respectfully requested.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870
Attorney of Record

Raymond F. Cardillo, Jr.
Registration No. 40,440

Customer Number
22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)

EHK:RFC:brf

(viii) CLAIMS APPENDIX

14. A semiconductor device comprising:

a semiconductor substrate;

a first impurity diffusion layer formed in the semiconductor substrate;

a second impurity diffusion layer formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer formed on the first impurity diffusion layer so as to cover the first impurity diffusion layer except for a tip portion opposite to the second impurity diffusion layer;

a second insulating layer formed on the second impurity diffusion layer so as to cover the second impurity diffusion layer except for a tip portion opposite to the first impurity diffusion layer;

a trench formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer;

a gate insulating film lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench, the gate electrode conductive layer being formed in an overlapped relation relative to the tip portion of the first impurity diffusion layer and the tip portion of the second impurity diffusion layer,

wherein the gate insulating film contains one selected from the group consisting of Ta_2O5, Al_2O_3, $BaSrTiO_3$, Zr oxide Hf oxide, Sc oxide, Y oxide, and Ti oxide.

15. The semiconductor device according to claim 14, wherein the gate insulating film is formed of an insulating material having a dielectric constant of above 5.

17. The semiconductor device according to claim 14, wherein the first impurity diffusion layer and the second impurity diffusion layer, each, comprise a third impurity diffusion layer forming a corresponding tip portion beneath the gate insulating film formed on the inner sidewall surface of the trench and a fourth impurity diffusion layer including a portion formed beneath a corresponding one of the first insulating layer and second insulating layer and having a deeper junction in the semiconductor substrate than the third impurity diffusion layer.

18. The semiconductor device according to claim 14, further comprising a metal silicide layer formed on the first impurity diffusion layer and the second impurity diffusion layer at those areas adjacent to the first insulating layer and the second insulating layer.

(ix) EVIDENCE APPENDIX

NONE

(x) RELATED PROCEEDINGS APPENDIX

NONE